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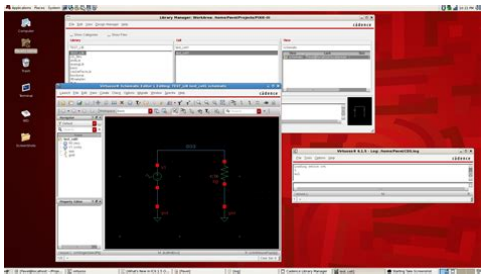

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The input should turn from. OFF to ON. CAUTION Cadence is very fragile concerning thisClick on Enabled, Function dc, Type Voltage, DC voltage 5. Source type dc, and click on Apply. The vdd! should turn from OFF to ON. Click OK.In this case we will choose tran which is the default, For small circuits as we have now itNow we can finally simulate. Click on the Netlist and Run button. Netlist and Run. Click OK on the Welcome to Spectre windowIn case you have errors you will need to go back and correct them. CAUTION EachAssuming there are no errors you can now admire the simulationNow you have to click on the signalsIn order to do this You should finally get the desired simulation results, 2 gloriousVTC for the inverter. For this we first need to replace the INChange its DC voltage property to 5Component as in Lab1, then the voltage source in the schematic,If you dont have any errorsCongratulations, this is the end of Tutorial 2. In this case, you may find helpful information to address your particular problem on the Agilent EEsof EDA Knowledge Center. You can access the Knowledge Center from the Agilent EEsof EDA Web site at If the simulator encounters a Spectre Analysis statement in the netlist, a warning message similar to the following will be reported Many of these control statements are not supported by RF Design Environment. The information below will help you understand some of the issues related to these control statements and how you might work around a particular situation. The Spectre altergroup statement is used to change model file parameters by listing the device, model, and circuit parameter statements as you would in the main netlist. If the simulator encounters a Spectre alter statement in the netlist, a

warning message is reported and the statement is ignored. If the simulator encounters a Spectre assert statement in the netlist, a warning message is reported and the statement is ignored.http://educationext.com/userfile/ford-escape-2001-xls-manual.xml

If the simulator encounters a Spectre check statement in the netlist, a warning message is reported and the statement is ignored. If the simulator encounters a Spectre checklimit statement in the netlist, a warning message is reported and the statement is ignored. If the simulator encounters a Spectre ic or nodeset statement in the netlist, a warning message is reported and the statement is ignored. The info statement enables you to access the values of input, output, and operatingpoint parameters in Spectre and print a capacitance table. If the simulator encounters a Spectre info statement in the netlist, a warning message is reported and the statement is ignored. If the simulator encounters a Spectre options statement in the netlist, a warning message is reported and the statement is ignored. If the simulator encounters a Spectre paramset statement in the netlist, a warning message is reported and the statement is ignored. If the simulator encounters a Spectre save statement in the netlist, a warning message is reported and the statement is ignored. If the simulator encounters a Spectre set statement in the netlist, a warning message is reported and the statement is ignored. If the simulator encounters a Spectre shell statement in the netlist, a warning message is reported and the statement is ignored. If the simulator encounters a Spectre paramtest component in the netlist, a warning message is reported and the statement is ignored. The scalem feature is not supported by RF Design Environment and there is no equivalent model scale factor in RFDE. The model scale factor is specified in the Spectre options statement. If a scalem statement is encountered, a warning message is generated and the options statement is ignored. If your device or model is not listed in the Supported Devices and Models section, the component or model should be considered unsupported.

Therefore, if you have a Spectre HDL model that you want to use, the recommendation is to convert your Spectre HDL model to a VerilogA model. If you attempt to netlist an HDL module, an error will be generated. If a CMI model is encountered, an error will be generated. In order to use CMI, the recommendation is to convert your CMI models to RFDE userdefined models or VerilogA models. The ADS documentation set can be accessed from the Agilent EEsof EDA Web site at If a Spectre encrypted model is encountered, an error will be generated. The recommendation is to use the spectrespp command to output a 100% Spectre syntax file and then use that file with RF Design Environment. The issue here is that the netlist must be 100% SPICE syntax. The nettrans command will not accept a netlist with a mix of Spectre and SPICE syntax. You can access this documentation from the Agilent EEsof EDA Web site at Any simulation that attempts to netlist an unsupported format will generate a syntax error. In general, any time the simulator encounters an error, the simulation will be terminated. See also the Agilent EEsof EDA Knowledge Center for the latest uptodate information. It meets the changing It meets the changing simulation needs of designers as they progress through the design cycle—from architecture exploration to analog and RF blocklevel development and to final analog and mixed signal fullchip verification. This approach advanced mixedsignal SoC. It accepts device model updates are available with delivers the performance and capacity for designs in combinations of hardware all the simulators at the same time.It is tightly integrated with the Virtuoso custom design platform and provides detailed transistorlevel analysis in multiple domains. All sweep types are supported The “Turbo”. All rights reserved. Cadence, the Cadence logo, Incisive, Spectre, Verilog, and Virtuoso are registered trademarks of Cadence Design Systems, Inc.

OSCI and SystemC are registered trademarks of the Open SystemC Initiative, Inc., in the U.S. and other countries and is used with permission. For these reasons, we usually use another SPICE simulator Hspice. Please go to HSpice Simulation page to use HSPICE. However, in case we need to use Spectre, here we go. At this point, you should have set up the environment. Otherwise, refer to

Setting Up Your Unix Environment. Click apply to generate a postscript file. They can be opened as Note that since most people are more familiar with SPICE syntax, perhaps that should be used. Also, this new example makes different simulations from the first one. Spectre is casesensitive. This provides a general outline, but be aware that every step does not need to be done for every analysis. Oftentimes, the default values are already set correctly and no action needs to be taken for that step. Detailed descriptions of the functions of all the controls are found in Help, accessed by selecting Sonnet Help from the Sonnet menu in the Cadence Virtuoso CIW, layout window or Sonnet's Cadence Virtuoso Interface main window. You may access specific topics in Help by clicking on the Help button in any dialog box in the Cadence Virtuoso Interface. For a detailed, step by step example, please see the tutorial. When "cell" is used in the Sonnet environment, it is referring to the smallest part of the analysis grid used in subsectioning your circuit. Once the Sonnet menu appears in the layout window, you select Sonnet Create SonnetEM view to open the Create SonnetEM view from Layout View dialog box which allows you to create the SonnetEM view. To open the interface after the SonnetEM view has been created, open the SonnetEM view in a layout window, load the Sonnet menu Launch Sonnet , then select Sonnet Open Interface Application to open the interface. The Cadence Virtuoso Interface main window, shown below, is used to perform the rest of the tasks in the design flow.

You use the Substrate File Setup dialog box, shown below, to control these settings. You open the dialog box by clicking on the Edit Substrate button in the Substrate section of the Cadence Virtuoso Interface. For a detailed explanation of the controls and settings, please click on the Help button in the Substrate File Setup dialog box or on the link above. Port connections are usually made at the box sidewalls. The substrate is on the metal bottom of the box and represents the ground plane. Above the substrate are stacked the dielectric layers and metal levels. The side walls of the box are modeled as lossless metal. The top and bottom of the box may be assigned any metal type defined in the geometry project. You open the dialog box by clicking on the Options button in the Analysis Box section of the Cadence Virtuoso Interface main window. For more information on the box, see Sonnet Box. You may enter an Adaptive Band Sweep ABS or list of frequencies directly in the main interface window, as pictured below. Other types of sweeps must be entered in the Frequencies dialog box opened by clicking on the More button in the Frequencies section of the interface. In that case, a message appears in the main interface directing you to the Frequencies dialog box. There are four different types of models available in the main interface window SParameters in Touchstone format, a Broadband Spice model in Spectre format, a NCoupled Line model, and an Inductor model. Additionally, you may select SParameters in Spectre format in the Advanced Model Options dialog box, opened when you click on the Options button. You may also choose to create no models at all. Virtuoso pins are converted to Sonnet ports. All pin types, with the exception of symbolic, may be used in Virtuoso when you are using Sonnet as your electromagnetic solver. Pins can be converted to standard boxwall ports, cocalibrated ports, delta gap ports, and via ports.

Clicking on the Add Pins button opens the Create Shape Pin dialog box and clicking on the Ports button opens the Ports dialog box. When a Pin is added, it is automatically converted to a Sonnet port. You may add the shape pins before creating the SonnetEm View or add them in the SonnetEm View using the Add Pins button. For more information on the Create Shape Pin dialog box, please refer to Cadence Virtuoso's help. To change the parameters of the ports, you click on the Ports button to open the Ports dialog box. For more information on ports and their parameters, please click on the Help button in the Ports dialog box, or on the link. Click on a port to select it and then click the Edit button to edit that port. The Edit Port dialog box appears. Clicking on the Options button opens the Analysis Options dialog box. Analysis Estimate memory subsections your circuit and estimates the memory required for the analysis. Analysis Estimate Box Resonances allows you to detect possible box resonances before running your simulation. Tools Check Connectivity opens your circuit in the project editor so that you can check for any opens or shorts in your circuit that might

have been created during the translation. In those cases, you can use the command Analysis Simulate and Release to run your analysis. There is also a complete log of your analysis run, as well as the ability to create automatic documentation for your analysis. For more information, see the Results menu for the Cadence Virtuoso Interface. The official Cadence documentation they provide a user guide and reference manual for every software package is a very good source of information, however sometimes it can appear a little overwhelming to the beginner since there are a lot of manuals and they are usually lenghty the workshop manuals instead focus on more specific topics e.g. LNA design and simulation and are really useful as a quick reference.

There is also the online documentation, accessible from the GUI or using the terminal; e.g. to get help on the Spectre TRAN simulation type spectre help tran Another very good resource is the Cadence forum. Below are two screenshots of the spreadsheets opened in LibreOffice Calc If a parameter is sweeped, e.g. source parameter voltage, current, impedance,., model parameter resistance, capacitance, physical dimension,. or temperature, it also finds the DC transfer curves. It is a largesignal analysis. NOTE components whose capacitance or impedance is frequencydependent e.g. transmission lines are substituted by Spectre with their equivalent capacitance or impedance calculated at the frequency you define in the analysis window default 1Hz.It assumes that the circuit can be represented with a linear timeinvariant model. NOTE In AC simulations the smallsignal input should be small enough that the circuit transfer function can be found using a linear timeinvariant model, in other words the circuit should not become nonlinear due to the input signal or better, the nonlinearity should be so small that it can be ignored. If in doubt you can always do a TRAN transient simulation to confirm that the circuit is working as it should. Like the AC analysis it is a smallsignal analysis. Note that it works differently compared to an AC simulation, which instead finds the transfer function from a single source to any node in the circuit.It firstly determines the fundamental frequency of the circuit, which is a multiple of all source frequencies the input sources need to be coperiodic; Then it evaluates the circuit for one period of the common frequency, adjusting this period untill all voltages and currents fall within a specified tolerance between 2 consecutive periods call this period Tperiod. This means that the steadystate is a periodically timevarying operating point with period equal to Tperiod.

This analysis is required by the periodic timevarying analyses like PAC, PXF, Pnoise. It is a largesignal analysis.NOTE Like AC simulations, PAC simulations work well when the smallsignal input is small enough that the circuit transfer function can be found using a linear model, in other words the circuit should not become nonlinear due to the input signal or better, the nonlinearity should be so small that it can be discarded. This does not apply to the large signals for example the local oscillator input in a mixer whose effects are taken into account during the linearization phase and then discarded during the smallsignal analysis. Before performing a PAC analysis, a PSS analisys is required. For example it simulates the noise at the output due to a noise source that is bias dependent, such that its noise is modulated due to the periodic timevariance of the operating point and transfer function.It is a largesignal analysis, however only one input must be defined as a large signal all the other inputs must be sinusoidal and smaller than that one moderate . You can select which signal is defined as large or moderate in the QPSS window see image on the right Use this analysis for circuits like switchedcapacitor filters and mixers, and circuits that have multitone frequency conversion effects.Before performing a QPAC analysis, a QPSS analisys is required. To be continued.To do this, create a file named.cdsplotinit in the home directory with this text Useful especially while using the parametric analysis tool, to plot e.g. the gm of a mosfet vs drain current The lock files have the same name as the open files but have the.cdslck extension. If Cadence crashes, the files that were open at the time would be still locked when it is restarted and, to continue working on those files, the edit locks the lock files need to be removed. To remove the lock files you can use the clsAdminTool utility from the terminal.

He studied electrical engineering at the University of California, Berkeley under professors Alberto SangiovanniVincentelli and Robert Meyer and received his doctorate in 1989. During this time, he created the Spectre circuit simulator. From 1989 to 2005 he was a Fellow at Cadence Design Systems during which time he was the principal architect of the Spectre circuit simulation family.Proceedings of the IEEE, vol. 95, no. 3, pp. 622639, March 2007. By using this site, you agree to the Terms of Use and Privacy Policy. This tutorial will go through a simple RLC Butterworth filter AC simulation. More examples will be added in the future. This output text file can then be postprocessed manually or via scripts. The ac analysis output file is then processed to determine the 3dB bandwidth and attenuation of the filter. This will help us to continuously improve the MSEE Microelectronics program. Thank you very much. It is capable of modifying circuit, Consequently Therefore they apply to all analyses Otherwise all The object is located within outerHierarchy a list of instances with If outerHierarchy is not given Because SPICE OPUS treats the hierarchical paths of all objects in the The available Colon is used as the separator between So m1x1x2 is an instance named m1 If what is a list of strings a multiple save directives are returned Because SPECTRE knows no such thing as vector parameters, index The name of the parameter can be specified with If parameter is temperature a sweep of the Otherwise the parameters are passed If it is not given If debug is above 2 full simulator output is printed. Setting it to If gain is given as This does not mean that any results were produced. It only means that the return code from the simuator was 0 OK. Finally the Its return value is stored in the If there are n jobs in the job list. This means we have n job groups with one job per job group.

Integer, real, and string simulator options are converted with the All parameters It is written to. When a user executes a program, the operating system creates an address space for it to run in. The JVM consumes additional memory, so the net memory available to. Contents. Chapter 1 Getting Started With PowerWorld. The later is computed from the celllevel performance measures of all the VCs that. Cadence Encounter. Top level integration. Synopsys Primetime. Timing estimation. Mentor Graphics Calibre. Extraction, LVS, DRC. Device library data. doc. Contains PDF and HTML formats of user guide jre. Java Runtime Environment. Sample Schedule 2013 B.S.E. Electrical Engineering. Terms. Ashley Tarokh and Kuang Yu Liu, for their technical comments. Additionally, we also model the.This statement grants you permission to print. Spectre Circuit Simulator User Guide. January 2004. 3. Product Version 5.0. Preface.. Calling Subcircuits. All rights reserved. Printed in the United States of America. Cadence Design Systems, Inc., 555 River Oaks Parkway, San Jose, CA 95134, USA Trademarks Trademarks and service marks of Cadence Design Systems, Inc. Cadence contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence’s trademarks, contact the corporate legal department at the address shown above or call 800.862.4522. All other trademarks are the property of their respective holders. Restricted Print Permission This publication is protected by copyright and any unauthorized use of this publication may violate copyright, trademark, and other laws. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. This statement grants you permission to print one 1 hard copy of this publication subject to the following conditions 1.

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explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information. Spectre is an advanced circuit simulator that simulates analog and digital circuits at the differential equation level. The simulator uses improved algorithms that offer increased simulation speed and greatly improved convergence characteristics over SPICE. Besides the basic capabilities, the Spectre circuit simulator provides significant additional capabilities over SPICE. Typographic and Syntax Conventions This list describes the syntax conventions used for the Spectre circuit simulator.These keywords represent command function, routine or option names, filenames and paths, and any other sort of typein commands. When used with ORbars, they enclose a list of choices.

Boston Kluwer Academic Publishers, 1995. You must choose one argument from the list.. Three dots . indicate that you can repeat the previous argument. If you use them with brackets, you can specify zero or more arguments. If they are used without brackets, you must specify at least one argument, but you can specify more. Important The language requires many characters not included in the preceding list. You must enter required characters exactly as shown. See Appendix A, “References,” of the Spectre Circuit Simulator Reference manual for more detailed information. The basic capabilities of the Spectre circuit simulator are similar in function and application to SPICE, but the Spectre circuit simulator is not descended from SPICE. The Spectre and SPICE simulators use the same basic algorithms—such as implicit integration methods, NewtonRaphson, and direct matrix solution—but every algorithm is newly implemented. Spectre algorithms, the best currently available, give you an improved simulator that is faster, more accurate, more reliable, and more flexible than previous SPICElike simulators. January 2004 16 Product Version 5.0 Spectre Circuit Simulator User Guide Introducing the Spectre Circuit Simulator Improvements over SPICE The Spectre circuit simulator has many improvements over SPICE. Improved Capacity The Spectre circuit simulator can simulate larger circuits than other simulators because its convergence algorithms are effective with large circuits, because it is fast, and because it is frugal with memory and uses dynamic memory allocation. For large circuits, the Spectre circuit simulator typically uses less than half as much memory as SPICE. Improved Accuracy Improved component models and core simulator algorithms make the Spectre circuit simulator more accurate than other simulators. The Spectre BSIM3v3 is a physicsbased metaloxide semiconductor field effect transistor MOSFET model for simulating analog circuits.

The Spectre models include the MOS0 model, which is even simpler and faster than MOS1 for simulating noncritical MOS transistors in logic circuits and behavioral models, MOS 9, EKV, BTAHVMOS, BTASOI, VBIC95, TOM2, HBT, and many more. Chargeconserving models The capacitancebased nonlinear MOS capacitor models used in many SPICE derivatives can create or destroy small amounts of charge on every time step. The Spectre simulator’s Fourier analyzer has greater resolution for measuring small distortion products on a large sinusoidal signal. Resolution is normally greater than 120 dB. Furthermore, the Spectre simulator’s Fourier analyzer is not subject to aliasing, a common error in Fourier analysis. The Spectre circuit simulator improves the control of local truncation error in the transient analysis by controlling error in the voltage rather than the charge. For other simulations, you might accept a slower simulation to achieve greater accuracy. With the Spectre circuit simulator, you can make such adjustments easily by setting a single parameter. Improved Speed The Spectre circuit simulator is designed to improve simulation speed. The Spectre circuit simulator can be over 10 times faster than SPICE when SPICE is hampered by discontinuity in the models or problems in the code. Occasionally, the Spectre circuit simulator is slower when it finds ringing or oscillation that goes unnoticed by SPICE. For example, the Spectre circuit simulator warns of models used in forbidden operating regions, of incorrectly wired circuits,

and of erroneous component parameter values. By identifying such common errors, the Spectre circuit simulator saves you the time required to find these errors with other simulators. You can obtain these circuits from the Microelectronics Center of North Carolina MCNC if you have File Transfer Protocol FTP access on the Internet. You can also get information about the performance of several simulators with these circuits.

The Spectre circuit simulator has successfully simulated all of these circuits. Sometimes the netlists required minor syntax corrections, such as inserting balancing parentheses, but circuits were never altered, and options were never changed to affect convergence. It also includes the temperature effects, noise, and MOSFET intrinsic capacitance models. The Spectre Compiled Model Interface CMI option lets you integrate new devices into the Spectre simulator using a very powerful, efficient, and flexible C language interface. This CMI option, the same one used by Spectre developers, lets you install proprietary models. To see how the Spectre circuit simulator is run under the analog circuit design environment, read the Cadence Analog Design Environment User Guide. You can also run the Spectre circuit simulator in the ComposertoSpectre direct simulation environment. With this system, you can find information about any parameter associated with any Spectre component or analysis. SpectreHDL is proprietary to Cadence and is provided for backward compatibility. The VerilogA language is an open standard, which was based upon SpectreHDL. The VerilogA language is preferred because it is upward compatible with VerilogAMS, a powerful and industrystandard mixedsignal language. Both languages use functional description text files modules to model the behavior of electrical circuits and other systems. Each programming language allows you to create your own models by simply writing down the equations. The AHDL lets you describe models in a simple and natural manner. This is a higher level modeling language than previous modeling languages, and you can use it without being concerned about the complexities of the simulator or the simulator algorithms. In addition, you can combine AHDL components with Spectre builtin primitives.